REQUEST FOR ADDITION OF NEW COURSE

OFFICE OF THE UNIVERSITY REGISTRAR

PROPOSED COURSE DESCRIPTION

<table>
<thead>
<tr>
<th>Rubric &amp; No.</th>
<th>EE 7241</th>
<th>Title</th>
<th>Nanoelectronics</th>
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</thead>
<tbody>
<tr>
<td>Short Title (≤ 19 characters)</td>
<td>N A N N O E L E C T R O N I C S</td>
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<tr>
<td>Semester Hours of Credit</td>
<td>3</td>
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<tr>
<td>If combination course type, # hrs. of credit for</td>
<td>Lecture: 3</td>
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<td>Repeat Credit Max. (if repeatable):</td>
<td>NA_credit hours</td>
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<td>Credit will not be given for this course and:</td>
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<td>Course Type (Indicate hours in the appropriate course type.)</td>
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<tr>
<td>Lecture</td>
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<tr>
<td>Lab</td>
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<td>Seminar</td>
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<td>Clin/Pract</td>
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<td>Intern</td>
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<td>Maximum enrollment per section: (use integer, e.g. 25 not 20-30)</td>
<td>30</td>
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<td>Grading System:</td>
<td>Letter Grade X</td>
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<td>Final Exam:</td>
<td>Yes X</td>
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<td><strong>(Attach justification if the proposed course will not hold a final exam during examination week.)</strong></td>
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Course Description:
(Concise catalog statement exactly as you wish it to appear in the General Catalog)

EE 7241 Nanoelectronics (3) Prerequisites: Credit or registration in EE4242 or permission of the instructor. Nanoscale Devices, Circuits and Integration.

BUDGET IMPACT (IF ANSWER TO ANY QUESTION IS "YES", ATTACH EXPLANATION.)

If this course is approved, will additional staff be needed? Yes No X
Will additional space, equipment, special library materials or other major expense be involved? Yes No X

Academic Affairs Approval: (Date)

ATTACHMENTS (ATTACH THE FOLLOWING TO YOUR PROPOSAL)

JUSTIFICATION: Justification must explain why this course is needed and how it fits into the curricula. Will the course duplicate other courses?
SYLLABUS: Including 14 week outline of the subject matter; titles of text, lab manual, and/or required readings; grading scale and criteria
(For 4000-level, specify graduate student grading criteria if requirements differ for graduate and undergraduate students.)

APPROVALS

Department Faculty Approval Date | 9/28/2017 | College Faculty Approval Date | 2/15/18

Department Chair Signature (date)
Graduate Dean Signature (date)

College Dean Signature (date)
Course Justification: Well-known Moore's Law is about to reach its scaling limits within a decade as predicted. There is global effort to find replacement of current silicon nm CMOS technology; 10nm and 7.5nm CMOS technologies are being pursued at commercial and R&D levels by major semiconductor chip manufacturing companies. In search of replacement of silicon-based nm CMOSFETs, non-classical devices based on emerging low dimensional novel materials and concepts are being explored. Nanoelectronics focused on nanoscale devices, circuits and integration is a unique integration of physics, chemistry, biology and engineering. There is no such course available to students in Electrical and Computer Engineering and students of other discipline across the campus.

Previous enrollment as a special topics course:

Fall 2017 – 8
Spring 2016 – 5
Spring 2013 - 11

Prepared by,

Ashok Srivastava
Date: February 5, 2018
Proposal for Converting a Special topics Course to a Catalog Course

EE7241: Nanoelectronics – Nanoscale Devices, Circuits and Integration

Catalog Data:

EE7200: Nanoelectronics (3) Prerequisites: EE4242 or Registration; or Permission of the Instructor. Nanoscale Devices, Circuits and Integration.

Pre-requisite by Topic:

CMOS transistors and circuits, device models, technology, integration and testability, classical and quantum mechanics and solid-state physics

Course Objectives and Learning Outcomes:

This course will focus on developing better understanding of emerging low dimensional novel materials such as carbon nanotubes, graphene and other than graphene based transistors and developing models for designing of ultra-low energy nanoscale-integrated electronic and nano-photonic circuits. The course will also cover other non-classical devices such as single electron transistors, spintronics, resonant tunneling devices, gate around silicon nanowires transistors, III-V material nanowire transistors, quantum dots and quantum-dot cellular automata and plasmonics. On-chip VLSI interconnect based on carbon nanotubes, graphene nanoribbon and hybrid materials will be introduced for possible replacement of copper interconnect in nm CMOS technologies.

With this background students can design integrated electronic circuits based on nanoscale devices for ultra-low power/energy operation and photonic integrated circuits including on-chip THz detectors. Students can design tiny chips with embedded sensors for biological and environmental sensing and biomedical circuits and systems.

Text and Additional Study Material:

Ashok Srivastava, Jose M. Marulanda, Yao Xu and Ashwani K. Sharma, Carbon-Based Electronics: Transistors and Interconnects at the Nanoscale. Pan Stanford Publishing, 2015; and Class Notes

References on current literature articles will be given in class.

Daniel Minoli, Nanotechnology Applications to Telecommunications and Networking, 2006 (John Wiley);

H.-S. Philip Wong and Deji Akinwande, Carbon Nanotube and Graphene Device Physics, 2011 (Cambridge University Press);

Niraj K. Jha and Deming Chen, Editors), Nanoelectronic Circuit Design, 2011 (Springer);

Rainer Waser (Editor), Nanoelectronics and Information Technology, 3rd Edition, John Wiley.
14 Weeks Course Outline:

1. Introduction to nanotechnology and business applications (0.5 week)
2. Nanotechnology Science – Physics (0.5 week)
3. Nanotechnology Science – Chemistry (0.5 week)
4. Nanotechnology Science – Quantum Physics (0.5 week)
5. FinFET based Nanoscale Integration and Design (0.5 week)
6. 2D Material Graphene and Other than Graphene 2D Materials (3 weeks)
   - Physical Properties
   - Mesoscopic Transport
   - Nanomaterial Processing
   - Devices, Circuits and Integration
7. Midterm (0.33 week)
8. 1D Carbon Nanotubes (3 weeks)
   - Physical Properties
   - Mesoscopic Transport
   - Nanomaterial Processing
   - Devices, Circuits and Integration
9. Other Non-Classical Devices (3 weeks)
   - Single Electron Transistors
   - Spintronics
   - Resonant Tunneling Devices
   - Gate Around Silicon Nanowire Transistors
   - III-V Material Nanowire Transistors
   - Quantum Dots and Quantum-Dot Cellular Automata
   - Plasmonics
10. CNT, GNR, and Hybrid Materials –based Interconnect (1.5 week)
11. Term Papers Presentation (0.67 week)

Grading:

30% Term Paper (Final Report and Short Presentation); 10% HW, Midterm (30%) and Final Exam (30%)

Grading Scale:

<table>
<thead>
<tr>
<th>Letter Grade</th>
<th>A+</th>
<th>A</th>
<th>A-</th>
<th>B+</th>
<th>B</th>
<th>B-</th>
<th>C+</th>
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<th>C-</th>
<th>D+</th>
<th>D</th>
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<td>90-</td>
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<td>84</td>
<td>80-</td>
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<td>70-</td>
<td>65-</td>
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<td>55-</td>
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<td>60-</td>
<td>55-</td>
<td>50-</td>
<td>45-</td>
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Note: Grading scale may change depending upon class average and performance.
Note: No Make-up test/exam will be given except for reasons in PS-22.
EE7200: Nanoelectronics – Nanoscale Devices, Circuits and Integration

Detailed Description of Activities that will be graded:

**Mid-term Exam:** A mid-term exam will be taken in class on the date mentioned in syllabus. No Make-up test/exam will be given except for legitimate medical reasons. Mid-term exam content will include the material covered before the set date of the exam. The midterm exam grade will be 30% of the 100% total grade.

**Final Exam:** A final exam will be taken at the time and date published in the LSU scheduling book. The content will cover material beyond the mid-term material and before the last date of the end of the class. The exam grade will be computed as 30% of the 100% of total grade.

**Homework:** Homework will be given after the end of subject covered as numbered in syllabus and will constitute 10% of 100% total grade.

**Term Paper:** Every student will be required to work on a term paper of scholarly in nature and well researched in emerging advanced topic of the field of nanoelectronics, make intermediate presentation during midterm and final presentation before the end of the class and submit term paper in required format. It will constitute 30% of the 100% total grade.

**Expectations:** LSU’s general policy states that for each credit hour, the student should plan to spend at least two hours working on course related activities outside of class. Since this course is for three credit hours, student should expect to spend a minimum of six hours outside of class each week working on assignments for this course.

**LSU Student Code of Conduct:** The LSU student code of conduct explains student rights, excused absences, and what is expected of student behavior. Students are expected to understand this code as described here: [http://students.lsu.edu/saa/students/code](http://students.lsu.edu/saa/students/code). Any violations of the LSU student code will be duly reported to the Dean of Students.

**Disabilities:** The course is in compliance with the American with Disabilities Act and the Rehabilitation Act of 1973, as amended and in accordance with the LSU policies as described under: [http://www.lsu.edu/students/disability/students/types-accommodations.php](http://www.lsu.edu/students/disability/students/types-accommodations.php).

**Academic Success:** The primary ingredients of your academic success are attending classes, managing your time efficiently, taking good notes, and developing good critical thinking and communication abilities.

The place to begin is the Center for Academic Success ([http://students.lsu.edu/academicsuccess](http://students.lsu.edu/academicsuccess)). The CAS offers guidance on what learning strategies are best suited to your talents, tutorial in the basic subjects, and workshops on a variety of topics, from note taking to time management. Finally, with respect to professional success, the LSU Online Career Center ([http://students.lsu.edu/careercenter](http://students.lsu.edu/careercenter)) can assist you in choosing a major and a profession that best suits your talents and passions and help you develop a career plan to ensure success when you graduate from LSU. Last but not the least an academic interaction with the professor and making best use of office hours can help you a lot for a successful professional career.
**Course Justification:** Well-known Moore’s Law is about to reach its scaling limits within a decade as predicted. There is global effort to find replacement of current silicon nm CMOS technology; 10nm and 7.5nm CMOS technologies are being pursued at commercial and R&D levels by major semiconductor chip manufacturing companies. In search of replacement of silicon-based nm CMOSFETs, non-classical devices based on emerging low dimensional novel materials and concepts are being explored. Nanoelectronics focused on nanoscale devices, circuits and integration is a unique integration of physics, chemistry, biology and engineering. There is no such course available to students in Electrical and Computer Engineering and students of other discipline across the campus.

Since fall 2013, this course has been offered three times in the current form, with an average enrollment of ~ 5-7.

Prepared by,

Ashok Srivastava
Date: February 5, 2018

Date Revised: March 26, 2018